Patent Claims

1. An address generator for generating addresses for testing an addressable circuit (2), having:
(a) at least one base address register (12) for buffer-storing a base address, the base address register (12) in each case being assigned an associated offset register group (13) having a plurality of offset registers for buffer-storing relative address values;
(b) a first multiplexer circuit (38), which, in a manner dependent on a base register selection control signal, switches through an address buffer-stored in the base address register (12) to a first input (59) of an addition circuit (60) and to an address bus (3), which is connected to the circuit (2) to be tested;
(c) a second multiplexer circuit (17), which, in a manner dependent on the base register selection control signal, through-connects the offset register group (13) associated with the through-connected base address register (12) to a third multiplexer circuit (25), which, in a manner dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group (13) to a second input (61) of the addition circuit (60);
(d) the addition circuit (60) adding the address present at the first input to the relative address value present at the second input (61) to form an address which is buffer-stored in the base address register (12).

2. The address generator as claimed in claim 1, characterized
in that the base address register (12) and the associated offset registers (13) can be initialized by an external test device (8), via initialization lines (10).

3. The address generator as claimed in claim 1 or 2, characterized
in that the address signal switched through to the address bus (3) can be inverted by a controllable inverting circuit (54).

4. The address generator as claimed in one of the preceding claims,
characterized
in that the number of offset registers of an offset register group (13) is equal to the number of address test jump variants required for testing the circuit (2).

5. The address generator as claimed in one of the preceding claims,
characterized
in that the circuit (2) to be tested is a synchronous RAM memory with a high operating clock frequency.

6. The address generator as claimed in one of the preceding claims,
characterized
in that the RAM memory has a multiplicity of memory cells which can be addressed via a multidimensional address space (X, Y).

7. The address generator as claimed in one of the preceding claims,
characterized
in that the number of base address registers (12) corresponds to the dimension (d) of the address space of the memory (2) to be tested.

8. The address generator as claimed in one of the preceding claims,
characterized

in that the base register selection control signals and the offset register selection control signals are applied to the address generator (1) by an external test device (8) via an address control signal bus (9),
the bus width of the address control signal bus (9) being less than the bus width of the address bus (3) of the circuit (2) to be tested.

9. The address generator as claimed in one of the preceding claims,
characterized
in that the line lengths of the address bus lines between the address generator (1) and the circuit (2) to be tested are smaller than the line lengths of the address control lines between the test device (8) and the address generator (1).

10. The address generator as claimed in one of the preceding claims,
characterized
in that the address generator (1) is integrated in the circuit (2) to be tested.